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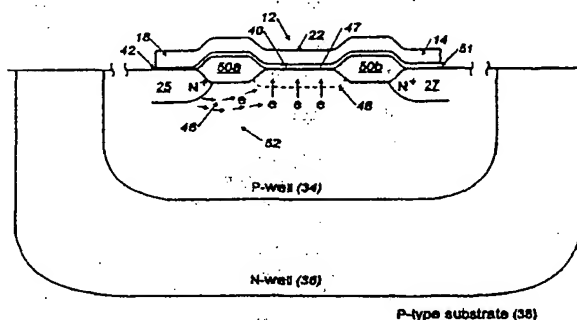
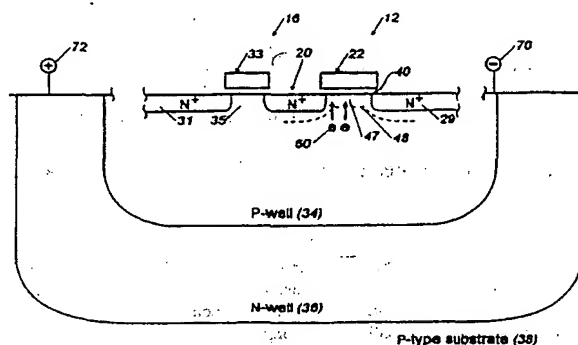
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(54) Title: NONVOLATILE MEMORY

## (57) Abstract

A nonvolatile memory cell is formed in an embedded P-well without the necessity of including an overlying control gate. As a result, normal logic process technology may be utilized to form the nonvolatile memory cell. Through the use of substrate hot electron injection and the formation of a lateral bipolar transistor whose emitter acts as a charge injector, programming efficiency is improved and the necessary programming voltages and currents can be reduced from the relatively high voltages and currents used in other devices.



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NONVOLATILE MEMORYBackground of the Invention

This invention relates generally to nonvolatile memories and particularly to electrically erasable nonvolatile memories.

Nonvolatile memory cells are advantageous since they retain recorded information even when the power to the memory is turned off. There are several different types of nonvolatile memories including erasable programmable read only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs) and flash EEPROM memories. EPROMs are erasable through light exposure but are electrically programmable by channel electron injection onto a floating gate. Conventional EEPROMs have the same programming functionality, but instead of being light erasable they can be erased and programmed by electron tunneling. Thus, information may be stored in these memories, retained when the power is off, and the memories may be erased for reprogramming, as necessary, using appropriate techniques. Flash EEPROMs are block erased, typically giving them better read access times than regular EEPROMs.

Currently, flash memories have gained considerable popularity. For example, flash memories are often utilized to provide on-chip memory for microcontrollers, modems and SMART cards and the like where it is desirable to store codes that may need fast updating.

While flash memories and EEPROMs are closely related, in many instances flash memories are preferred because their smaller cell size means that they can be made more economically. However, flash memories and EEPROMs often have very similar cell attributes.

Nonvolatile memory cells differ in certain respects from the transistors that are generally utilized in

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electronic components called logic devices, such as micro-controllers, that work with the memory cells. Logic devices are formed of transistors that use a single gate electrode. Nonvolatile memories usually include two gate electrodes,  
5 known as the control and floating gate electrodes, situated one over the other. Because of this structural difference, nonvolatile memories and logic devices may be made by different processes. This may contribute to a substantial increase in process complexity and manufacturing cost.

0 Particularly with an EEPROM, the electrical programming of the cells normally requires substantial potentials to be applied to the cells. These potentials induce electron tunneling from an N+ region onto the floating gate. Additional complexity may arise from the need to provide substantially larger voltages to memory cells than are needed for normal transistor operation.

While the industry has come to accept the need for separate process technologies for logic and nonvolatile memories and while those in the industry have also come to  
20 appreciate that significant voltages are needed to program EEPROMs and significant currents to program flash EEPROMs, there would be a substantial demand for a nonvolatile memory which was both electrically erasable and programmable without the need for special process  
25 technologies or for relatively higher programming voltages and higher currents.

Furthermore, with the conventional FLASH EEPROMs, the electrical programming of the cells normally requires high current to be applied to the cells. A relatively  
30 minute amount of this electron current becomes injected from the drain depletion region onto the floating gate. Therefore, the injection efficiency (e.g.,  $10^{-6}$  to  $10^{-9}$ ) is relatively low. The requirement of high current adds additional complexity because of the design of the high  
35 current pump operated at low voltage.

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Summary of the Invention

In accordance with one aspect of the present invention, an electrically erasable and programmable read-only memory includes a sensing cell with a floating gate electrode, a channel, a source and a drain. A bipolar transistor is adapted to supply electrons for programming the floating gate electrode by substrate hot electron injection of electrons on to the floating gate electrode through the channel depletion region. The bipolar transistor is arranged such that its collector is also the biased depletion region of the channel of the sensing cell.

In accordance with still another aspect, a nonvolatile memory includes a semiconductor layer of a first conductivity type. A first well of a second conductivity type opposite to the first conductivity type is formed in the semiconductor layer. The first well is an N-well biased to a potential equal to or more positive than  $V_{ss}$ . A second well of the first conductivity type is embedded in the first well. The second well is a negatively biased P-well. A memory cell is formed in the second well. The cell includes a floating gate, a source and a drain. The source and drain are of the second conductivity type.

In accordance with yet another aspect of the present invention, a memory cell includes a semiconductor layer having a N-well. A P-well is embedded in the N-well. The sense transistor has a floating gate and a bipolar transistor arranged to inject electrons into the substrate. The injected (pump) electrons can be accelerated by the electric field under the sense transistor channel and get injected onto the floating gate.

In accordance with yet another aspect of the present invention, a method for programming a memory cell includes the step of turning off a select transistor. Carriers are

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caused to be injected onto the floating gate by substrate hot carrier injection.

In accordance with still another aspect of the present invention, a method for programming a memory cell includes the step of generating substrate electrons using a bipolar transistor. Substrate electrons are accelerated by the electric field under the channel and are injected onto the floating gate of the memory cell. These accelerated electrons are called substrate "hot" electrons.

10 In accordance with but another aspect of the present invention, a method for forming a memory cell includes the step of forming a floating gate over a channel in a substrate. A diffusion is formed in the substrate spaced from the channel underneath the floating gate and extending  
15 under the floating gate. A source and drain are formed for the cell, arranged substantially transversely to the length of the floating gate.

In accordance with another aspect of the present invention, a nonvolatile memory comprises a sense transistor  
20 having a floating gate. A coupling capacitor is formed at one end of the floating gate. The coupling capacitor is arranged to control the potential on the floating gate. The floating gate is free of an overlaying control gate electrode. A tunneling capacitor is formed at another end  
25 of the floating gate. The tunneling capacitor provides a path for electrons to be removed from the floating gate. It also acts as part of a charge injector for supplying electrons to the channel region under the sense transistor. The tunneling capacitor includes a junction forming the  
30 emitter of a lateral bipolar transistor, the biased depletion region of the sense transistor channel under said floating gate acting as the collector of the lateral bipolar transistor.

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Brief Description of the Drawing

Figure 1 is a schematic depiction of one embodiment;

Figure 2 is a top plan view showing the layout of a semiconductor implementation of the embodiment shown in Figure 1;

Figure 3 is a cross-sectional view taken generally along the line 3-3 in figure 2;

Figure 4 is a cross-sectional view taken generally along the line 4-4 in figure 2; and

Figure 5 is a schematic depiction of an array configuration for the cell shown in Figure 1.

Description of the Preferred Embodiment

Referring to the drawing wherein like reference characters are used for like parts throughout the several views, a memory cell 10, shown in Fig. 1, includes a tunneling capacitor 18, a sense transistor 12, a select transistor 16, and a coupling capacitor 14. This structure is advantageously implemented on a semiconductor layer having situated thereon an electrically isolated floating gate 22.

The tunneling capacitor 18 is controlled by the flash node 24, and the coupling capacitor 14 is controlled by the control node 28. The drain 29 of the sense transistor 12 is connected to the drain node 26 and the source 31 of select transistor 16 is connected to the source node 30. The gate 33 of the select transistor 16 is connected to the select node 32.

One layout for implementing the cell 10, shown in Fig. 2, includes the flash node 24 which is implemented as a contact and a diffusion 25 which is typically an N-type diffusion. The floating gate 22 extends over the diffusion 25 to define the tunneling capacitor 18. Similarly, the floating gate 22 extends over the diffusion 27 to define the coupling capacitor 14. The control node 28 for the

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coupling capacitor 14 may be implemented by a contact, as shown in Fig. 2.

The drain node 26 may include a contact as illustrated in Fig. 2 which connects to a diffusion 29.  
5 The source node 30 may be implemented by a contact as illustrated. The source of the sense transistor 12 and the drain of the select transistor 16 are common as indicated at 20 in Fig. 2. The gate electrode of the select transistor 16 is formed as the conductive layer 33 which  
10 connects to a contact (not shown). A single pair of a source 30 and drain 26 contacts are operative to form two transistors with separate gates 22 and 33.

The relationship of the sense transistor 12 and select transistor 16 is illustrated in Figure 3. The  
15 floating gate 22 forms the gate of a transistor having a drain 29 and a common junction 20. Similarly, the gate 33 acts to control conduction between the source 31 and the common junction 20. The sense transistor 12 includes a channel 47 while the select transistor 16 includes a  
20 channel 35. In the illustrated embodiment, the channels 47 and 35 are P-type semiconductor material and are part of a P-well 34. The P-well 34 in turn is formed in an N-well 36. Finally, the N-well 36 is formed in a P-type substrate 38. The P-well may be negatively biased, as indicated at  
25 70, and the N-well 36 may be positively biased, as indicated at 72. The N-well 36 may be biased to a potential equal to or more positive than  $V_{ss}$ .

Referring now to Figure 4, the configuration of the floating gate 22 in connection with the tunneling capacitor  
30 18 and coupling capacitor 14 can be explained. The floating gate 22 extends over a pair of field oxide regions 50 which extend generally parallel to the source-to-drain direction of the sense transistor 12 and select transistor 16. At one end in Figure 4, the floating gate 22 forms the  
35 tunneling capacitor 18 by its interaction with the



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underlying region 25 which may be an N<sup>+</sup> diffusion. A tunneling oxide 42 separates the floating gate 22 from the diffusion 25. Similarly the gate oxide 40 separates the floating gate 22 from the channel 47. Finally, the floating gate 22 is separated by the oxide 51 from the diffusion 27 of the coupling capacitor 14. Thus, the floating gate 22 is part of the sense transistor 12 and the capacitors 14 and 18.

The cell 10 may be described as a flash EEPROM utilizing high efficiency substrate hot electron injection for programming and Fowler-Nordheim tunneling for erasure. The process of substrate hot electron injection is well described in T. H. Ning, C. M. Osburn, and H. W. Yu "Emission Probability of Hot Electrons from Silicon into Silicon Dioxide", J. Appl. Phys., vol. 48, p.286, (1977); Boaz Eitan, James L. McCreary, Daniel Amrany, Joseph Shappir, "Substrate Hot-electron Injection EPROM", IEEE Transactions on Electron Devices, Vol. ED-31, No. 7, p.934, (July 1984); I. C. Chen, C. Kaya, and J. Paterson, "Band-to-Band Tunneling Induced Substrate Hot-electron (BBISHE) injection: A New Programming Mechanism for Nonvolatile Memory Devices", IEDM (1989) p.263; and C. Y. Hu, D. L. Kencke, S. K. Benerjee, "Substrate-current-induced Hot Electron (SCIHE) Injection: A New Convergence Scheme for FLASH Memory," IEDM (1995), p.283. Each of these articles is hereby expressly incorporated by reference herein.

Programming is achieved by high efficiency substrate hot electron injection. As indicated in Figure 4, substrate electrons, indicated at 60, are generated by forward biasing the diffusion 25 which is separated from the sense transistor 12 by the field oxide 50a. Some of the substrate electrons 60 diffuse through the region underneath the field oxide 50a to the channel region 47 underneath the sense transistor 12. For cells that need to be programmed, the channel region 47 is biased such that a

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depletion region 48 is formed. When an electron gets to the depletion region 48, it is accelerated by an electric field,  $V_{cs}$ , which is the difference between the channel 47 potential (potential of the surface inversion region) and the P-well 34 potential. Some of these electrons gain sufficient energy, in excess of the effective oxide barrier height potential, to be injected onto the floating gate 22. For cells that are not to be programmed, the channel-to-P-well potential is less than the effective oxide barrier height. In such case, the electrons would not gain sufficient energy to overcome the barrier height and are not injected onto the floating gate 22.

The diffusion 25, the P-region under the field oxide 50a and the biased depletion region 48 under the sense transistor 12 form a lateral bipolar transistor 62. The bipolar transistor 62 acts as a charge injector, injecting substrate electrons from the diffusion 25 onto the floating gate 22. With the diffusion 25 as the emitter, the P-region under the field oxide 50a as the base, the collector is the depletion region 48. The depletion region 48 is controlled by the  $N^+$  source 20 and  $N^+$  drain 29, and the P-well 34 potential. Since the channel region 47 acts as the channel for reading the sense transistor 12 and as the collector of the bipolar transistor 62 during programming, a compact cell layout is achieved.

The efficiency of substrate hot electron injection is a function of a number of characteristics. Considering the depletion region 48, electrons scatter with lattice phonon scattering across the depletion region 48 with a certain electron mean free path. Some of these electrons, without much scattering, gain sufficient energy to overcome the effective barrier height and are injected onto the floating gate 22. Some electrons gain less energy than the effective barrier height and are not injected onto the floating gate 22. The injection efficiency is a strong

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function of the doping concentrations and the channel-to-P-well potential,  $V_{cs}$ .

Since the cell 10 is situated in a P-well 34 embedded in an N-well 36, during programming the floating gate 22 is capacitively coupled to a higher voltage through the coupling capacitor 14 by raising the diffusion 27 to  $V_{pp}$ , which may be from 7 to 14 volts. The voltage that the floating gate 22 attains is a function of the voltage on the floating gate when both the nodes 24 and 28 are at ground, plus the coupling ratio times the voltage on the node 28. The coupling ratio to first order is approximately equal to the capacitance of the capacitor 14 divided by the sum of the capacitances of the coupling capacitor 14, the tunneling capacitor 18 and the capacitance between the floating gate 22 and the channel region 47.

When the select transistor 16 is off, the sense transistor drain 29 potential can be forced close to the supply potential  $V_{cc}$  or higher. Since the select transistor 16 is off, the source 20 potential follows the channel 47 potential. The channel 47 potential is the potential of the surface inversion region of the channel region. When the potential of the floating gate 22 is one sense transistor 12 threshold voltage higher than the drain 29 potential, the channel potential is the same as the drain potential. On the other hand, when the floating gate 22 potential is less than the drain 29 potential plus the sense transistor 12 threshold voltage, the channel potential is the difference between the floating gate 22 voltage and the sense transistor 12 threshold voltage.

The well potential is the voltage 70 applied to the P-well 34. Since the P-well is embedded in an N-well 36, and the N-well is set at a voltage 72 approximately  $V_{ss}$  or higher, the P-well potential  $V_p$  can be biased negatively, typically negative one to negative two volts. Moreover, it

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is usually less than the effective oxide barrier height to avoid any potential disturb problem.

The potential difference between the channel 47 region and the P-well 34 potential ( $V_p$ ) 70 is the voltage across the depletion region 48. For cells to be programmed, the drain 29 voltage is raised high, typically close to  $V_{cc}$ . A depletion region 48 in the channel 47 underneath the sense transistor 12 is formed with a voltage drop equal to the channel potential minus the P-well potential 70.

For those cells that are not to be programmed, the drain voltage 29 is set to zero volts. The voltage drop across the depletion region 48 then is equal to the absolute value of  $V_p$ , which is typically less than the effective oxide barrier height.

Cell 10 erasure is achieved by Fowler-Nordheim tunneling from the floating gate 22 to the node 24. The node 24 is therefore called the flash node. During erasure, the floating gate 22 is capacitively coupled through the capacitor 14 to a potential close to ground by forcing the diffusion 27 to ground. As for the diffusion 25, it is charged to a positive potential ( $V_{pp}$ ) of from 7 to 14 volts. The voltage across the capacitor 18 is the difference between the floating gate 22 potential and the diffusion 25 potential. When the difference exceeds 8 to 10 volts, sufficient tunneling current is generated and the floating gate 22 can be erased to a negative potential in the time frame of a few milliseconds to a few seconds, depending on the tunneling oxide 42 thickness.

Reading the programming state of the cell 10 may be accomplished as follows. For the selected row the floating gate 22 is capacitively coupled to a higher potential by forcing the diffusion 27 to a potential of 1.8 to 5 volts. The floating gate 22 is coupled to a potential  $V_{fg}$  which can be calculated as being equal to the sum of the floating

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gate potential when both nodes 24 and 28 are held at ground, plus the potential on the control node 28 times the coupling ratio.

The drain 29 potential during reading is limited to a voltage of less than 2 volts. This is to avoid any read disturb.

For the selected cell to be read, the select node 32 is forced to Vcc, and the source node 30 is forced to ground. The unselected gates 33 and the nodes 28, 30 and 32 are also forced to ground. The unselected column 26 is also forced to ground.

When these potentials are applied to the selected cell, a current flows through the sense transistor 12. This current is then fed to a current sense amplifier (not shown). If the voltage on the floating gate 22 is greater than the threshold voltage on the sense transistor 12, and a higher current, perhaps greater than 20 microamps flows, the cell state is detected as the conducting state. When the potential of the floating gate is less than the threshold voltage, a lower current, for example or less than one microamp flows, and a nonconducting state is detected.

A detected conducting state can be called a one state. A nonconducting state can be called the zero state.

The operation of the cell in programming, reading and erasing, for an exemplary embodiment, is summarized in the following example:

#### Cell Operation

		Erase
		Read
		(Selected)
(Unselected)	(Select)	(Unselected)
(Select)	(Unselected)	



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Vs is the node voltage set by the injection current level, ranging from a few nanoamps to a few tens of microamps depending on the programming speed requirement. Typically it would be from tens of milliseconds to tens of  
5 microseconds. Vbias is the bias on the P-well 34 which can be Vss or it can be forced to -1 to -2 volts to enhance injection efficiency. A suitable on-chip circuit for generating two negative bias potentials, one to bias the diffusion 31 and the other to negatively bias the P-well 34, can be found in L.A. Glasser and D.W. Dobberpuhl, "The Design and Analysis of VLSI Circuits", (Dec. 1985), published by Addison-Wesley, at pages 301-329, hereby expressly incorporated by reference herein. Vss is the external ground potential.

While the cell 10 may be utilized as a single element as shown in Fig. 1, it can also be connected as an array as shown in Fig. 5. In the array, a plurality of cells 10, 10a, 10b, 10c, 10d and, 10e are depicted. The flash node 24 is formed by connecting all of the flash  
20 nodes of cells in the same row as one single node. This enables all cells on the same row to be erased and programmed at the same time.

The control node 28 is formed by connecting all the control nodes of the individual cells in the same row  
25 together as a single node. This enables the floating gate 22 for all cells on the same row to rise to a relatively high potential (Vpp) during programming, such as 7-14 volts, at the same time and close to Vcc during read. All cells on the same row (which can be byte wide or page wide)  
30 can then be programmed together.

The source node 36 is formed by connecting the source lines for all the cells on the same row together. Similarly, the select gate node 32 can be formed by

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connecting together all the cells of the same row as a single node.

The drain node 26 is formed by connecting all the drain nodes for cells in the same column together as a single node. This node leads to the sense amplifier (not shown).

The cells in the array maybe formed using conventional process technologies such as a single poly, double metal process. Because there is no control gate electrode, a process technology that is completely compatible with normal logic process technology may be utilized.

The illustrative parameters set forth herein contemplate a  $.35\mu\text{m}$  or higher feature size with Vcc potentials of 2.7 volts or higher. As the technology permits lowering voltages and smaller feature sizes, the parameters herein would scale accordingly.

The starting substrate material is typically P-type (100) silicon, for example having a resistivity range of 10-25 ohm-cm. The P-well 34 is embedded in an N-well 36 in the so-called triple well process. The P-well 34 has a typical well depth of, for example, 2 to 4  $\mu\text{m}$  with an average doping concentration, for example, in the range of  $1 \times 10^{16}$  to  $5 \times 10^{16}$  atoms per cubic centimeter.

The N-well has a typical well depth of, for example, 4-8  $\mu\text{m}$ . The doping concentration may be from  $4 \times 10^{15}$  to  $1 \times 10^{16}$  atoms per cubic centimeter. The triple well is formed by the P-well 34 counterdoping the N-well 36.

The formation of the elements in the triple well is as follows. An N-well implant is done, for example, with phosphorous ( $\text{P}_{31}$ ) with a typical dose of  $1.0$  to  $1.5 \times 10^{13}$  atoms per square centimeter and energies from 160Kev to about 100Kev. The N-well implant is driven using a high temperature step which may typically be 6 to 12 hours at 1125 to 1150° C. The N-well 36 is then counterdoped with



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a P-well implant. Typical dosages for the P-well implant could be  $1.5$  to  $2.5 \times 10^{13}$  atoms per square centimeter with energies of 30Kev to 180Kev using a species such as boron (B11).

5       The N-well 36 and P-well 34 are then driven, typically 6 to 10 hours at 1125 to 1150° C. This sets the wells to the desired doping concentrations and depths.

After well formation, standard logic field oxide formation and channel stop formation steps are applied.  
10       The field oxide 50 and implant doses are adjusted to achieve a field threshold of 7 to 14 volts, which is determined by the Vpp level for programming and erasing and by logic process capability. After field oxide and channel stop formation, the N+ diffusions 25 and 27 are formed  
15       using an ion implant, such as a phosphorus implant, with an energy of 30-60 Kev and a dose of  $1.2 \times 10^{14}$  to  $2.5 \times 10^{14}$  atoms per square centimeter. This may be followed by an anneal cycle of 925 to 1000° C for 15 to 35 minutes.

After the formation of the N+ diffusions 25 and 27,  
20       the gate oxide 40 and the tunnel oxide 42 are formed. For example, a 70 to 90A dry oxide may be grown across the wafer followed by a resist masking step. The resist may cover everything except the tunnel oxide 42 region and the periphery N channel and P channel regions. The N and P  
25       channel threshold adjustment implants are then done into all the areas that are not covered by resist. A buffered oxide etch (BOE) is used to etch off the oxide in the region that is not covered by resist. After resist removal, a dry oxide is grown to a thickness 85 to 100  
30       Angstroms, for example, at 900° C in partial oxygen followed by a 975 to 1050° C anneal. This forms a gate oxide 40 with a typical thickness of 120 to 150 Angstroms and a tunnel oxide 42 of 85 to 100 Angstroms.

The floating gate 22 may then be formed of  
35       polysilicon, silicide or metals after the oxide 40 has been

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grown. Standard gate patterning is used and source/drain implant steps follow the gate patterning. This sequence forms two capacitors and two transistors. The tunnel oxide 42 is sandwiched between two electrodes, the N+ diffusion 25 and the floating gate 22. This forms the tunneling capacitor 18. The gate oxide 40 sandwiched between the floating gate 22 and the N+ diffusion 27 forms the coupling capacitor 14. The gate oxide 40 that is sandwiched between the floating gate and the channel region 47 forms the sense transistor 12. The select transistor 16 is formed by the gate oxide 40 and the select gate 33.

With the completion of these capacitor and transistor structures, all subsequent processing for contacts and interconnect layers follows standard logic rear end processing.

While a number of parameters and levels were provided in the foregoing description, those skilled in the art will appreciate that these parameters and levels are merely for illustration purposes. For example, by reversing the conductivity types of the doped junctions and the bias polarities, a cell structure using substrate hot hole injection may be implemented. It is intended that the appended claims cover all modifications and variations as fall within the true spirit and scope of the present invention.

What is claimed is:

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1. An electrically erasable and programmable read only memory comprising:

a sensing cell including a floating gate electrode, a channel, a source and a drain; and

5 a bipolar transistor adapted to supply electrons for programming said floating gate electrode by substrate hot carriers injection of carriers onto said floating gate electrode through said channel, said bipolar transistor arranged such that its collector is also the biased  
10 depletion region under the channel of said sensing cell.

2. The memory of claim 1 wherein said floating gate electrode is the only gate electrode for the sensing cell.

3. The memory of claim 2 including a select  
15 transistor.

4. The memory of claim 3 wherein said select transistor and said sense transistor share a common junction.

5. The memory of claim 1 wherein said floating  
20 gate electrode defines a sense transistor and a pair of capacitors.

6. The memory of claim 5 wherein said floating gate electrode also extends over a pair of doped regions and forms a coupling capacitor and a tunneling capacitor.

25 7. The memory of claim 1, wherein the emitter of said bipolar transistor is forward biased during programming.

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8. A nonvolatile memory comprising:

a semiconductor layer of a first conductivity type;

a first well in said semiconductor layer, said first well being of a second conductivity type opposite to said first conductivity type, said first well being an N-well biased to a potential equal to or more positive than  $V_{ss}$ ;

a second well being of said first conductivity type and embedded in said first well, said second well being a negatively biased P-well; and

10 a memory cell formed in said second well, said cell including a floating gate, a source and a drain, said source and drain being of said second conductivity type.

9. The memory of claim 8 wherein said floating gate is the only gate electrode for said cell.

15 10. The memory of claim 9 wherein said floating gate extends over a pair of regions of said second conductivity type to form a pair of capacitors, one of said capacitors arranged to define the erase path for said cell, and the other of said capacitors arranged to apply a  
20 potential for reading said cell.

11. A memory cell, comprising:

a semiconductor layer having an N-well;

a P-well embedded in said N-well; and

a sense transistor having a floating gate and a  
25 bipolar transistor arranging to inject electrons for hot electron injection onto said floating gate.

12. The cell of claim 11 wherein said P-well is biased negatively.

13. The cell of claim 11 including a select  
30 transistor, a coupling capacitor and a tunneling capacitor.

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14. The cell of claim 13 wherein said capacitors are formed at the opposed ends of said floating gate over N-type regions in said semiconductor layer.

15. The cell of claim 11 wherein the collector of said bipolar transistor corresponds to a biased depletion region of the the channel of said sense transistor.

16. The cell of claim 11 wherein said floating gate is the only gate electrode for said cell.

17. A method for programming a memory cell comprising the steps of:  
turning off a select transistor; and  
causing carriers to be injected onto a floating gate by substrate hot carrier injection.

18. The method of claim 17 including the step of forming said select transistor in a P-well and biasing said P-well negatively.

19. The method of claim 17 wherein said select transistor drain voltage is at least approximately the supply voltage.

20. The method of claim 17 wherein said carriers are electrons.

21. The method of claim 17 including the step of operating said floating gate without using an overlaying control gate.

22. The method of claim 21 including the step of using a capacitor formed from said floating gate to control the operation of said cell.

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23. A method for programming a memory cell having a channel comprising the steps of:

generating substrate electrons with a bipolar transistor; and

5 injecting said electrons onto the floating gate of said memory cell using substrate hot electron injection through said channel.

24. The method of claim 23 wherein said cell is formed in a P-well embedded in an N-well, said method  
10 including the step of biasing said P-well negatively.

25. The method of claim 23 including the step of turning off a select transistor.

26. The method of claim 25 including the step of controlling the operation of said floating gate without  
15 using an overlying control gate.

27. The method of claim 26 wherein said floating gate forms a capacitor with an underlying diffusion, said method including the step of controlling said floating gate using said capacitor.

20 28. The method of claim 23 including the step of forward biasing the emitter of a bipolar transistor used to provide a source of electrons for substrate hot electron injection.

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29. A method for forming a memory cell comprising the steps of:

forming a floating gate over a channel in a substrate;

5 forming a diffusion in said substrate spaced from said channel underneath said floating gate and extending under said floating gate; and

forming a source and drain for said cell arranged substantially transversely to the length of said floating  
10 gate.

30. The method of claim 29 including the step of forming a pair of capacitors associated with the ends of said floating gate.

31. The method of claim 30 including the step of  
15 forming a select transistor having a common junction with said source of said cell.

32. The method of claim 31 including the step of forming said cell without providing a control gate over said floating gate.

20 33. The method of claim 29 including the step of forming said cell in a P-well embedded in an N-well.

34. The method of claim 33 including the step of providing for negative biasing of said P-well.

35. The method of claim 29 including the step of  
25 forming a field oxide region on one side of said cell.

36. The method of claim 35 including the step of forming lateral bipolar transistor extending under said field oxide region.

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37. The method of claim 36 including the step of forwarding biasing the emitter of said bipolar transistor for programming.

38. A nonvolatile memory comprising:

- 5 a sense transistor having a floating gate;  
a coupling capacitor formed at one end of said floating gate; said coupling capacitor arranged to control the potential on said floating gate, said floating gate being free of an overlaying control gate electrode; and  
10 a tunneling capacitor formed at another end of said floating gate, said tunneling capacitor providing a path for electrons to be removed from said floating gate and acting as part of a charge pump for supplying electrons to be injected onto said floating gate, said tunneling  
15 capacitor including a junction forming the emitter of a lateral bipolar transistor, said sense transistor channel biased depletion region under said floating gate, arranged to act as the collector of said lateral bipolar transistor.

39. The memory of claim 38 including a select  
20 transistor having a common junction with said sense transistor.

40. The memory of claim 39 wherein said sense transistor has a source and drain of a first conductivity type, said sense transistor being formed in a first well of  
25 a second conductivity type, said first well being formed in a second well of said first conductivity type.

41. The memory of claim 40 wherein said first conductivity type is N-type and said second conductivity type is P-type and said first well being negatively biased  
30 and said second well being positively biased.



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42. The memory of claim 38 wherein said tunneling capacitor junction being forward biased for programming.

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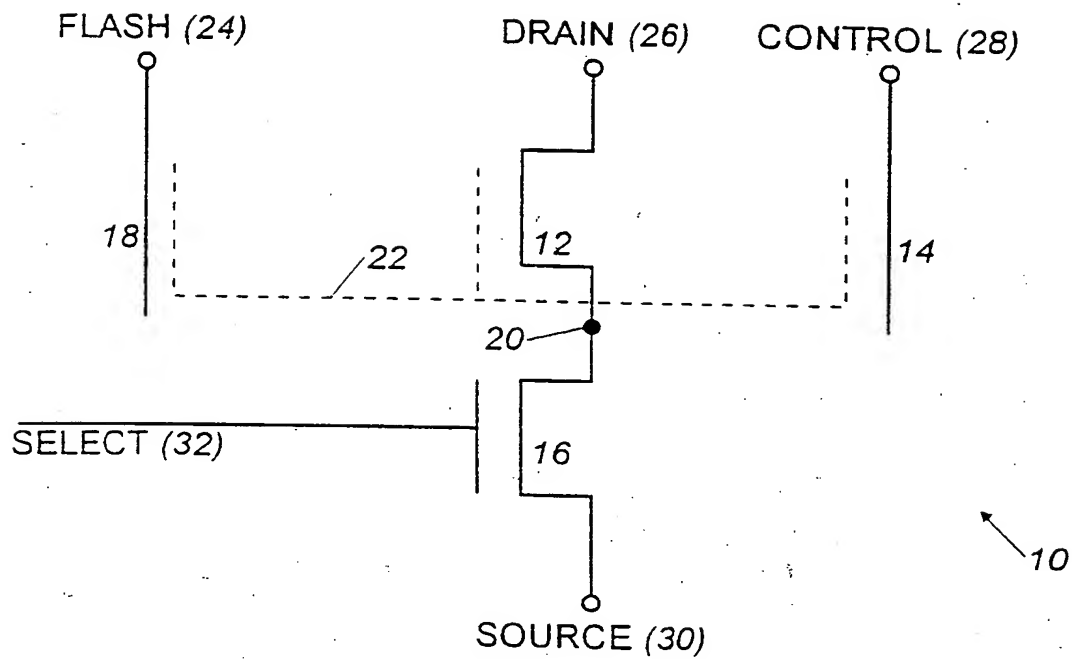


FIG. 1

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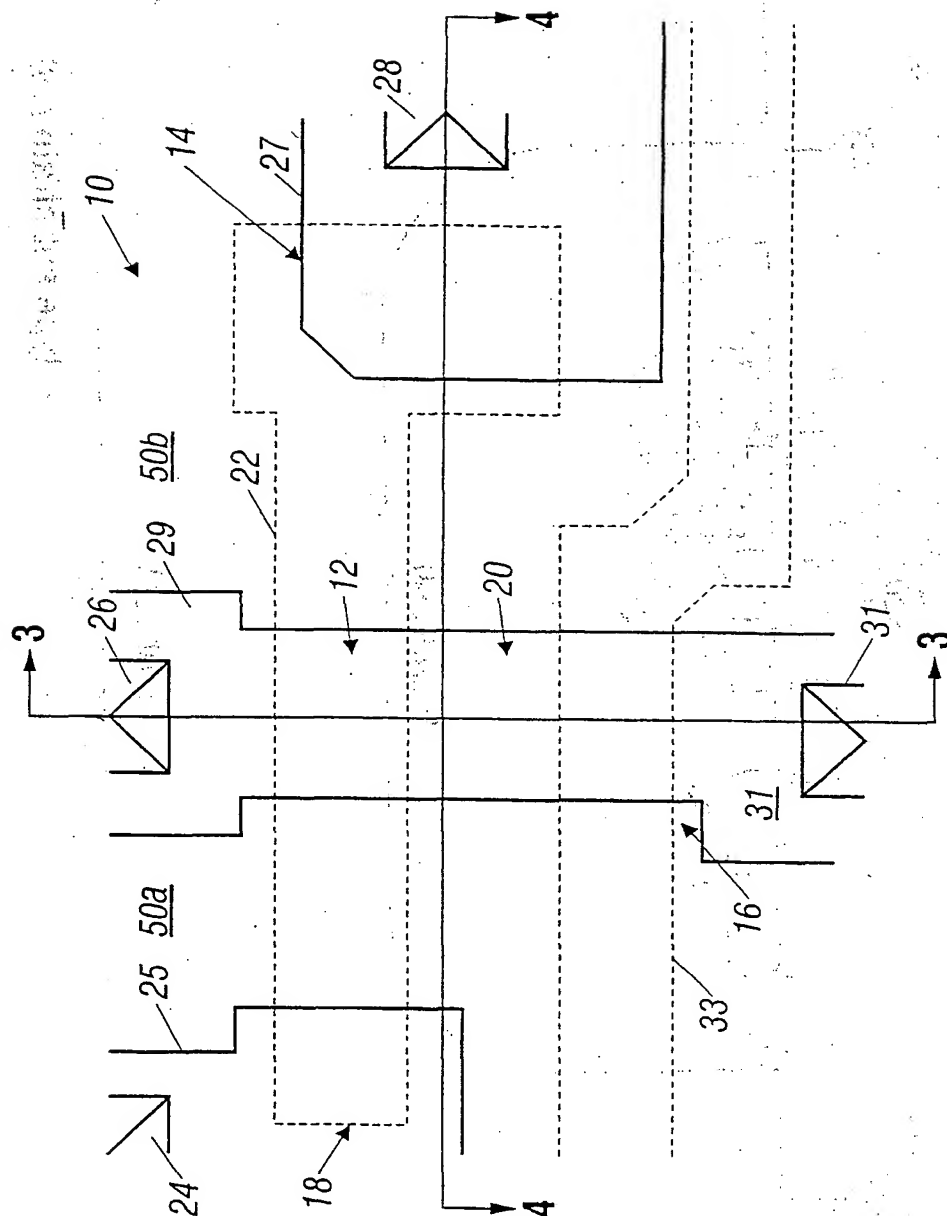


FIG. 2

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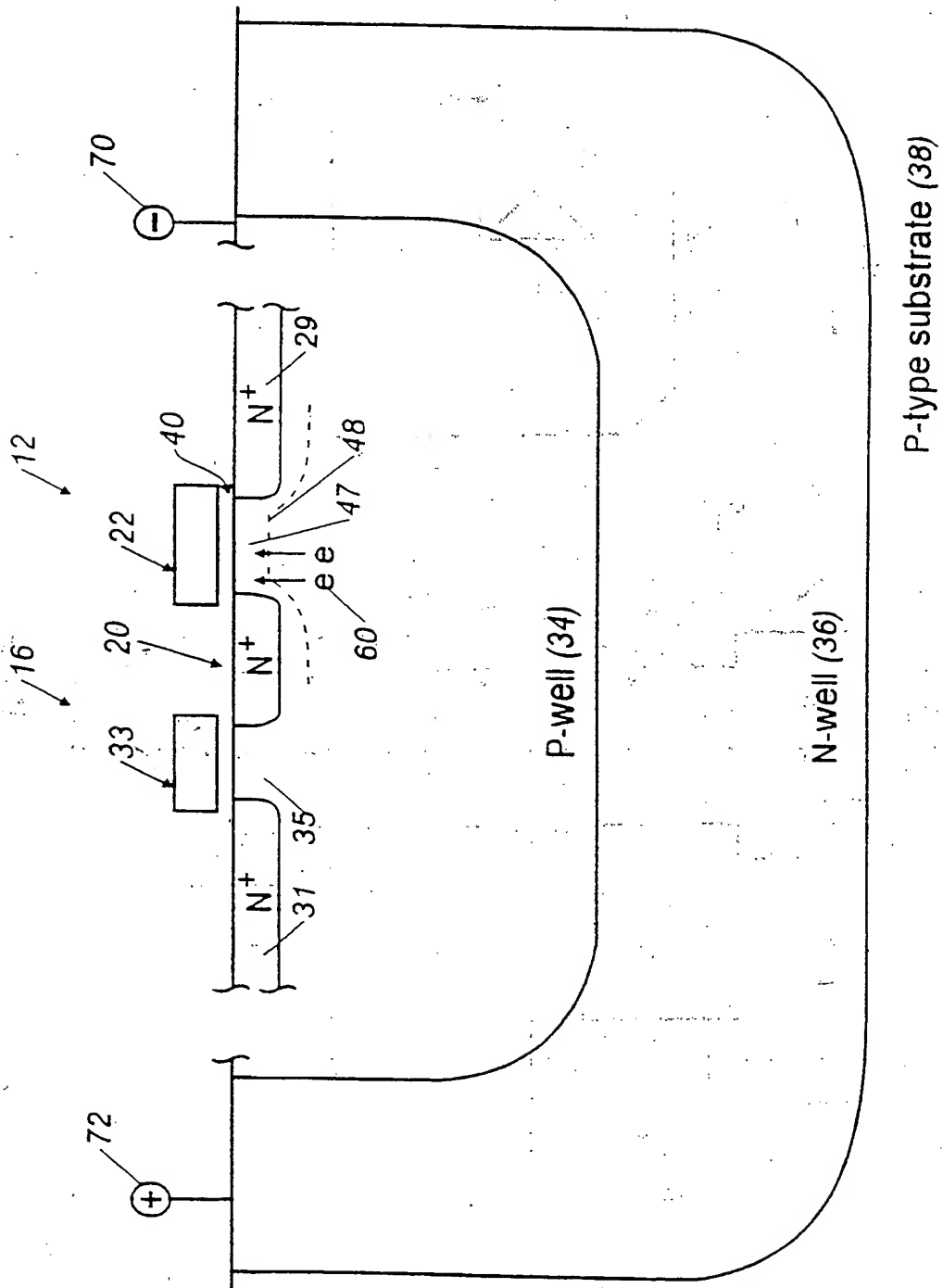
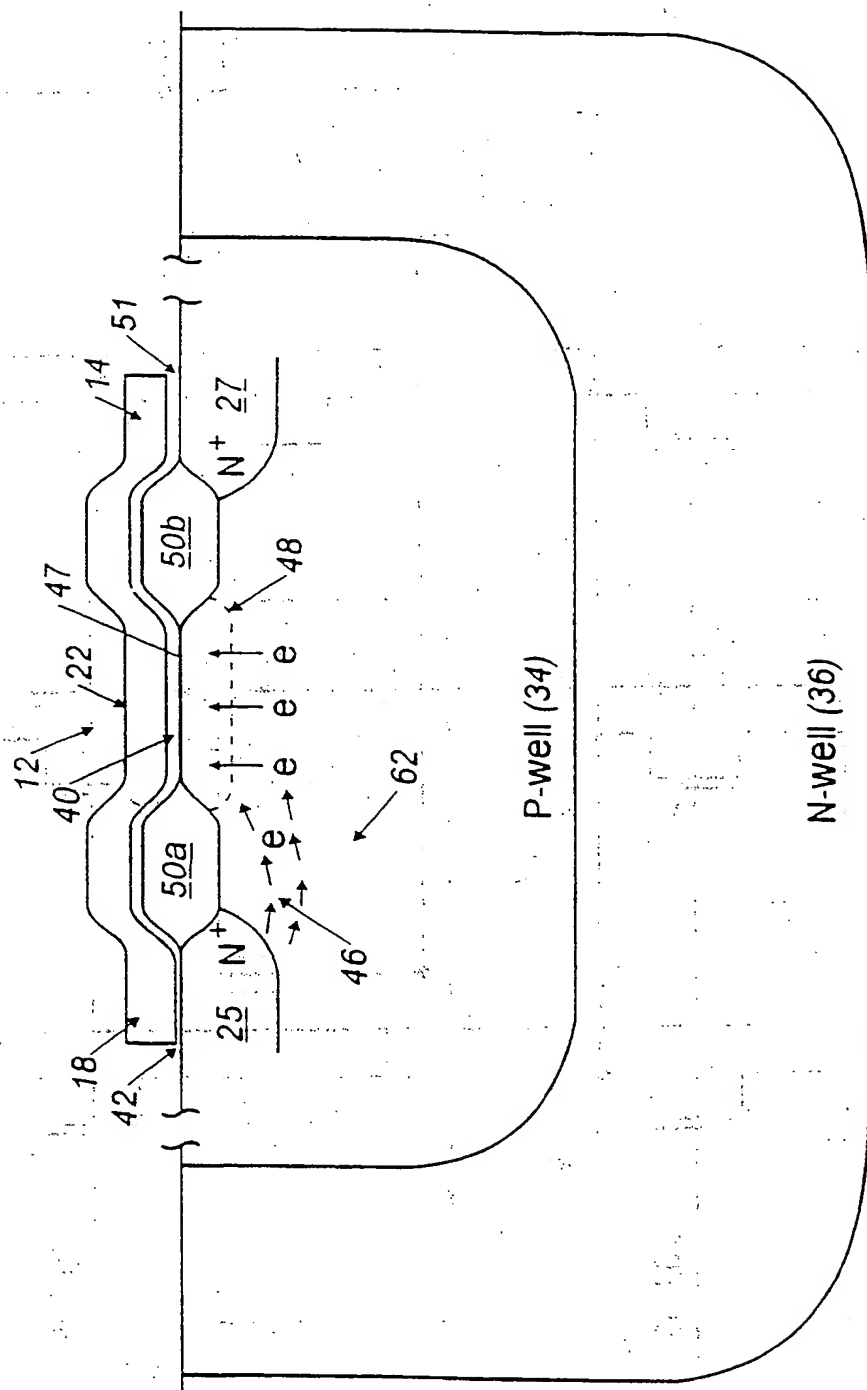


FIG. 3

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P-type substrate (38)

FIG. 4

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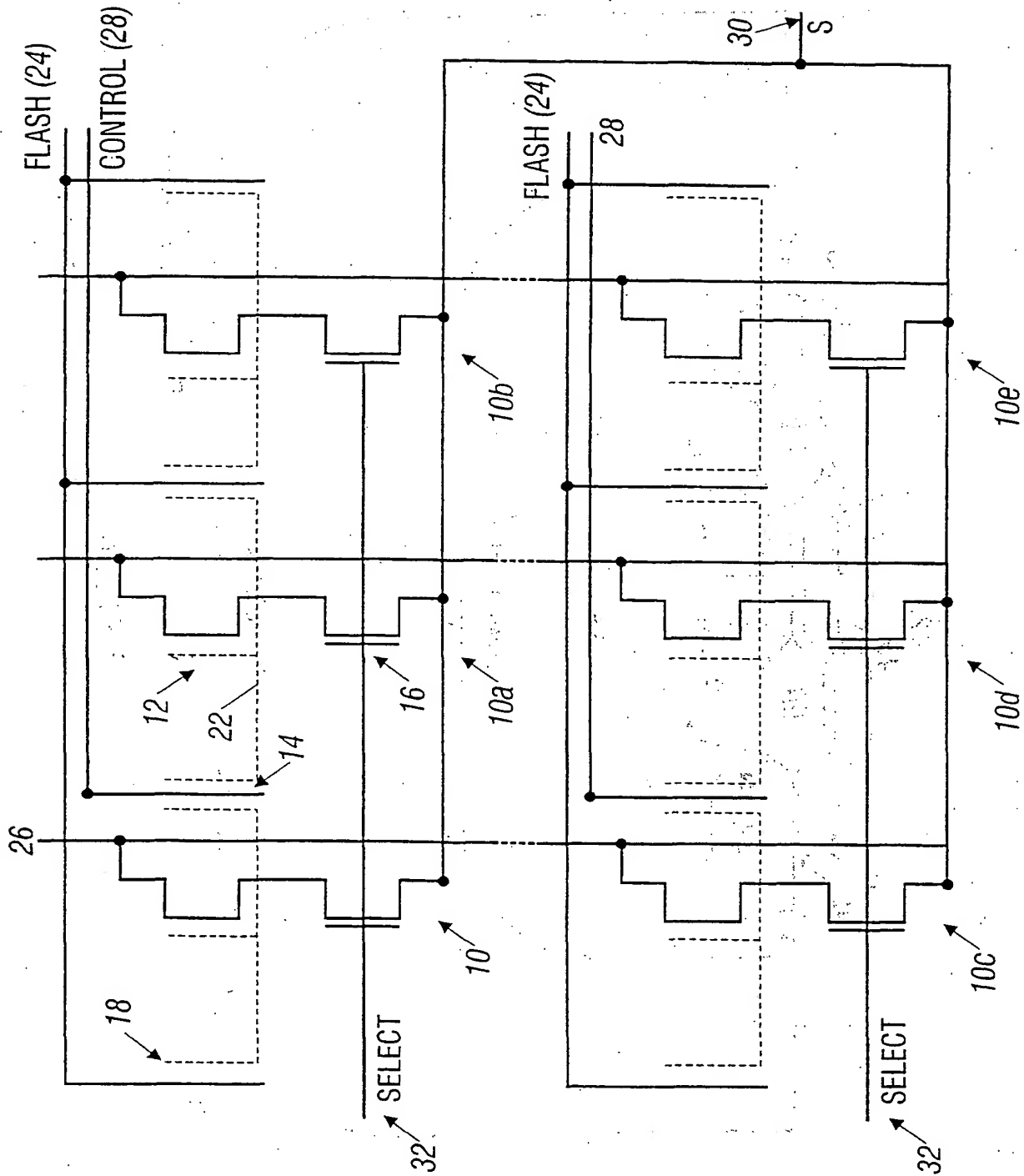


FIG. 5

# INTERNATIONAL SEARCH REPORT

national Application No

PCT/US 98/06777

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G11C16/04 H01L29/788

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G11C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TW 285 777 A (PROGRAMMABLE MICROELECTRONICS CORP.) 11 September 1996 & EP 0 776 049 A (PROGRAMMABLE MICROELECTRONICS CORP.) 28 May 1997	17, 29-32, 35
Y	see page 10, line 5 - page 13, line 57; figures 15-25 see page 3, line 28 - page 3, line 55; figures 1-4	10, 33, 37
X	US 5 301 150 A (SULLIVAN STEPHEN F ET AL) 5 April 1994	17-22
Y	see column 2, line 44 - column 3, line 28; figures 1-5 see column 5, line 5-41 see column 7, line 45 - column 8, line 27 -/-	33, 37



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

17 July 1998

Date of mailing of the international search report

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# INTERNATIONAL SEARCH REPORT

national Application No  
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